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then forming a dielectric layer covering the first surface of the silicon wafer and the via holes with distal portions of the dielectric layer being located at the bases of the via holes, so that the distal portions are closest to the reverse surface,

then forming metal vias in the via holes on the dielectric layer with proximal ends being located at the first surface and distal ends of the metal vias being located on the distal portions of the dielectric layer, thereby being closest to the reverse surface,

then forming an interconnection structure including multilayer conductor patterns over the metal vias and the dielectric layer,

then forming a protective overcoat layer composed of polyimide over the interconnnection structure,

then forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure leaving the reverse surface of the wafer exposed,

then thinning the reverse surface of the wafer to a desired thickness to form an Ultra Thin Silicon Wafer (UTSW) for the SBP exposing the distal portions of the dielectric layer covering the distal ends of the metal vias, and

then removing the distal portions of the dielectric layer exposing the distal ends of the metal vias which extend through the UTSW.

28. The method of claim 27 including:

forming the temporary bond with polyimide, and

releasing the temporary bond by laser ablation.

REMARKS

The claims have been amended in view of the Office action and in view of the remarks which follow, they are believed to be in condition for allowance.

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Claim Rejections - 35 USC§ 102(e)

On page 3 of the Detailed Action, claims 1-3 and 14 were rejected under 35 U.S.C. 102(e) as being anticipated by Siniaguine (US 6,184,060). The Office Action stated as follows:

> Siniaguine (Fig 2, 7, 8) discloses a method comprising starting with a wafer (104,110) composed of silicon and a reversed surface that which are planar as the base for a silicon based package, SBP, forming an interconnection structure including multiplayer [sic] conductor patterns (Column 2; Lines 27-29) over via and dielectrics, forming a temporary bond between the SBP and an inherent rigid wafer holder (Column 1, Lines 52-53),"

What is stated at Col. 1, lines 52-53 is as follows:

"In some embodiments, the wafer is held by a non-contact wafer holder during the back side etch. The face side of the wafer does not physically contact the holder."

Thus it is believed to be clear that the Siniaguine reference fails to claim what is defined by the amended claims where it is clear that the holder is bonded to the protective overcoat layer on the face side, i.e. the "first surface", of the wafer.

The Office Action stated further, as follows:

> "thinning the wafer to a desired thickness (Column 2, Lines 37) to form an ultra thin silicon wafer, UTSW (110, Fig 8A), forming via holes (130) which extend through the UTSW such that the base, and forming metallization or metal vias (150) in the via holes by bonding the metallization in the via extending through the UTSW; forming capture pads (180) prior to thinning the wafer (shown in Fig 7); with the capture pads being formed on the first surface and then forming the interconnection structure over the first surface and capture pads (Fig 9); inherently providing a base for a silicon package; with via holes that extend partially through the wafer from the first surface towards the reverse surface with each via hole having a base closest to the reverse surface (Fig 7) forming a dielectric layer (140) covering the first surface of the silicon wafer and the via holes with distal portions of the dielectric being located at the bases of the via holes so that the distal ends are closed to the reverse surface and metal vias having distal end on dielectric (150C) removing distal ends of dielectric layer (Fig 8A, 140a) exposing the distal ends of the metal vias which extend through the UTSW (Fig (8A).

In view of the amendments to the claims, the above rejection is now believed to be moot since elements are missing from the prior art as indicated in the above remarks.

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Claim Rejections - 35 USC§ 103

On page 4 of the Detailed Action, under 35 U.S.C. 103(a) claims 4 -13 and 16 were rejected as being unpatentable over Siniaguine as applied to claims 1 and 14. The Office Action stated as follows:

> "Siniaguine does not appear to disclose varying the claimed order of steps such as forming capture pads then forming interconnection then forming temporary bond of a wafer holder then thinning the wafer then forming vias holes, in any case, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed sequence because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. Moreover, it is well established that, in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959)."

As stated above it is clear that the Siniaguine reference fails to claim what is defined by the amended claims where it is clear that the holder is bonded to the protective overcoat layer on the face side, i.e. the "first surface", of the wafer, unlike Siniaguine. Moreover, the reference fails to deal with the problem of the extreme fragility of a UTW. By definition, a UTW, is ultra thin and therefore extremely fragile requiring great care in handling. It is because of the fragility of the process of Siniaguine that applicants developed a way to support the wafer until it can be assembled with a carrier body which supports it sufficiently to avoid damage which would otherwise be likely. The references to fragility of the UTW are found. This is added to the fact that the sequence of steps in claims 1-13 and new claims 25 and 26 are extremely different in that the via holes are not formed until late in the process, which avoids the probability of damage to the fragile wafers. At page 4, lines 13-20 the problem of breaking of fragile membranes thin substrates and wafers is mentioned. At page 5, lines 13-14 use of sacrificial glass plates as holders for ultra thin wafers is mentioned as solution provided by the instant invention to a serious handling problem in the manufacture of UTWs. At page 12, one 4-8, the provision of a glass wafer holder for temporary support of an ultra-thin wafer is mentioned as a means for permitting normal handling. The same idea is mentioned at page 20, lines 12-

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18 mentioning that the glass wafer holder supports a "fragile ultra-thin wafer" to permit normal handling. This is manifestly an unobvious solution to the problem of avoiding damage to wafers mentioned by Siniaguine who required use of a special "*non-contact wafer holder during the back side etch*... where the... *face side of the wafer does not physically contact the holder*". Moreover Sinanguine provided no subsequent support for very thin, fragile wafers, which would require extraordinary handling care to be exercised to avoid breaking wafer such as the highly valuable UTWs of this invention.

> "Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Siniaguine as applied to claim 14 in combination with Houston et al. (US 2002/0086519)."
>
> "Siniaguine does not appear to disclose forming a blanket of metal over dielectric layers including via holes followed by planarizing the blanket down to the surface of the dielectric layer forming metal vias in the via holes."
>
> "Houston (Fig 1 D,E) utilizes a method of forming a blanket of metal (24) over dielectric layers (14) including via holes (20) followed by planarizing the blanket down to the surface of the dielectric layer (par.0024)."
>
> "It would have been obvious to one of ordinary skill in the art to form metal in the vias of Siniaguine in the alternate process of forming a blanket of metal over dielectric layers including via holes followed by planarizing the blanket down to the surface of the dielectric layer in order to form a metal vias that is able to be coupled to an interconnect element as taught by Houston (Par. 0024)."

As stated above it is clear that the Siniaguine reference fails to claim what is defined by the amended claims where it is clear that the holder is bonded to the protective overcoat layer on the face side, i.e. the "first surface", of the wafer. Moreover, the sequence of steps in claims 1-13 and new claims 25 and 26 are extremely different in that the via holes are not formed until late in the process. The basic reference fails to suggest what is now the subject matter of the amended claims even when combined with Houston.

In Siniaguine, since the vias are etched first and filled they must be deep and that leads to a high aspect ratio. With the present invention as shown in FIGS. 2A-2M the viais etched after the wafer has been thinned down which is a process that facilitates filling of a shallower hole which can be done more reliably. In any event the provision of a bond to a temporary rigid mechanical support for the thin wafer is a concept unsuggested by Siniaguine who relies upon suspending the wafer in a technique that was not describe but

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based upon the literature may have involve use of a flow of gases in the etching chamber to suspend the work piece therein like a ball supported upon a fluid flow. Whatever the non--contacting process, it would be very complicated and require sophisticated processing techniques and complicated processing apparatus . Moreover it does not resolve the problem of handling the wafer after it has been etched.

Attached hereto is a "version of amendments to the specification and/or claims with markings to show changes made".

In view of the amendments and the above remarks favorable action including allowance of the claims and the application as a whole are respectfully solicited.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend the paragraph [0007] beginning at page 3, line 1 to read as follows:

- -[0007] U.S. patent No. 6,184,060 of Siniaguine for "Integrated Circuits and Methods for Their Fabrication" describes **formation of vias and** contact **pads** [~~vias formed~~] on the back side of a silicon semiconductor chip. The vias **and contact pads** are formed by the process starting with forming tapered vias (openings) in the back of a workpiece comprising a silicon wafer by with an isotropic plasma etch of the via opening down into the silicon wafer through an aluminum or photoresist mask formed over the silicon. The via opening**s have** [~~has~~] a depth at least as large as the final thickness of the wafer after the manufacturing process is completed. After the mask is removed, a thin conformal, glass or BPSG dielectric layer (1-2 μm thick) is formed over the substrate including the vias. Then a thin conformal blanket conductive layer (e.g. 0.8-1.2 μm thick) is formed over the dielectric layer of aluminum, gold or nickel. A planar glass layer is spun onto the surface of the conductive layer to fill the vias to provide a planar top surface of the wafer. The conductive layer may or may not have been patterned before the last step of filling the vias with the planar glass layer. Other layers to be a part of the device structure are then formed on top of the planarized surface of the workpiece including a dielectric layer and contact pads. Then the back side of the silicon wafer is etched by an atmospheric plasma etch with argon and carbon tetrafluoride in air. When the glass or BPSG dielectric layer becomes exposed**, the** silicon substrate is preferentially etched relative to the silicon dioxide **dielectric** layer by almost an order of magnitude difference with the silicon etching far more quickly. [The] **Thus, the portions of the** lower surface (back side) of the **conductive layer formed in the** via **opening**s comprise contact pads for the back side of the chip **which are exposed by the preferential etching away of the silicon**. - -

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Please amend the paragraph [0010] beginning at page 4, line 13 to read as follows:

-- [0010] One of the problems with using silicon based structures for electronic packaging applications is to be able to provide a highly reliable product by employing an efficient method of forming vias through a membrane thin silicon substrate, i.e. from the bottom surface through the silicon to the top of the silicon where the wiring structure is fabricated. [~~The~~] **That** requires forming the vias without breaking the fragile membrane thin wafer and yet performing the task with a highly competitive manufacturing cost. - -

IN THE CLAIMS

1. **(Amended)** A method for fabricating a silicon based package (SBP) [~~comprising~~] **in the sequence as follows**:

[~~start~~] **starting** with a wafer composed of silicon and having a first surface and a reverse surface which are planar as the base for the SBP,

then forming an interconnection structure including multilayer conductor patterns over the first surface,

then forming a protective overcoat layer over the interconnnection structure,

then forming a temporary bond between the **protective overcoat layer of the** SBP and a wafer holder, with the wafer holder being a rigid structure,

then thinning the **reverse surface of the** wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP,

then forming via holes which extend through the UTSW, and

then forming metallization in the via holes with the metallization extending through the UTSW.

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14. (Amended) A method for fabricating a silicon based package (SBP) comprising:

providing a base for the SBP comprising a wafer composed of silicon and having a first surface and a reverse surface which are planar,

then forming via holes which extend partially through the wafer from the first surface towards the reverse surface with the each via hole having a base thereof which is closest to the reverse surface,

then forming a dielectric layer covering the first surface of the silicon wafer and the via holes with distal portions of the dielectric layer being located at the bases of the via holes, so that the distal portions are closest to the reverse surface,

then forming metal vias in the via holes on the dielectric layer with proximal ends being located at the first surface and distal ends of the metal vias being located on the distal portions of the dielectric layer, thereby being closest to the reverse surface,

then forming an interconnection structure including multilayer conductor patterns over the metal vias and th e dielectric layer,

then forming a protective overcoat layer over the interconnnection structure,

then forming a temporary bond between the **protective overcoat layer of the** SBP and a wafer holder, with the wafer holder being a rigid structure leaving the reverse surface of the wafer exposed,

then thinning the **reverse surface of the** wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP exposing the distal portions of the dielectric layer covering the distal ends of the metal vias, and

then removing the distal portions of the dielectric layer exposing the distal ends of the metal vias which extend through the UTSW.

Cancel claims 17-24 without prejudice to prosecution thereof in a divisional application.

Add the following claims:

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25. A method for fabricating a Silicon Based Package (SBP) in the sequence as follows:

starting with a wafer composed of silicon and having a first surface and a reverse surface which are planar as the base for the SBP,

then forming an interconnection structure including multilayer conductor patterns over the first surface,

then forming a protective overcoat layer composed of polyimide over the interconnnection structure,

then forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure,

then thinning the reverse surface of the wafer to a desired thickness to form an Ultra Thin Silicon Wafer (UTSW) for the SBP,

then forming via holes which extend through the UTSW, and

then forming metallization in the via holes with the metallization extending through the UTSW.

26. The method of claim 25 including:

forming the temporary bond with polyimide, and

releasing the temporary bond by laser ablation.

27. A method for fabricating a silicon based package (SBP) comprising:

providing a base for the SBP comprising a wafer composed of silicon and having a first surface and a reverse surface which are planar,

then forming via holes which extend partially through the wafer from the first surface towards the reverse surface with the each via hole having a base thereof which is closest to the reverse surface,

then forming a dielectric layer covering the first surface of the silicon wafer and the via holes with distal portions of the dielectric layer being located at the bases of the via holes, so that the distal portions are closest to the reverse surface,

then forming metal vias in the via holes on the dielectric layer with proximal ends being located at the first surface and distal ends of the metal vias being located on the distal portions of the dielectric layer, thereby being closest to the reverse surface,

then forming an interconnection structure including multilayer conductor patterns over the metal vias and the dielectric layer,

then forming a protective overcoat layer composed of polyimide over the interconnnection structure,

then forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure leaving the reverse surface of the wafer exposed,

then thinning the reverse surface of the wafer to a desired thickness to form an Ultra Thin Silicon Wafer (UTSW) for the SBP exposing the distal portions of the dielectric layer covering the distal ends of the metal vias, and

then removing the distal portions of the dielectric layer exposing the distal ends of the metal vias which extend through the UTSW.

28. The method of claim 27 including:

forming the temporary bond with polyimide, and

releasing the temporary bond by laser ablation.